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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,925	07/28/2003	Lee M. Nicholson	YOR920030173US1	7501

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Paul D. Greeley, Esq.
Ohlandt, Greeley, Ruggiero & Perle, L.L.P.
10th Floor
One Landmark Square
Stamford, CT 06901-2682

EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,925	NICHOLSON ET AL.	
	Examiner	Art Unit	
	Hung Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) *32-50* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 15-31* is/are rejected.

7)☒ Claim(s) *10-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/28/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Invention of Group I, Claims 1-31, in the reply filed on 10/18/04 is acknowledged. The traversal is on the ground(s) that the search relating to an electrical interconnect structure will necessarily produce art relating to a method of preparing the electric interconnect structure so that examination of the claims of Group I and Group II would not be burdensome. This is not found persuasive because it is well settled that related inventions are restrictable if it is shown that these inventions distinct. It was clearly established that Group I and II inventions are in fact distinct.

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 32-50 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected Invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 10/18/04.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9, 15-19, 21 and 25-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Yew et al. (PN 6,265,780).

Yew et al. discloses, as shown in Figure 2E, an electrical interconnect structure on a substrate, comprising:

a first low k or ultra low k dielectric layer (204,212);

a low k CMP protective layer (206,214) disposed on the first low k dielectric layer;

a hardmask/CMP polish stop layer (208,216).

With regard to claims 2 and 5, the terms "CVD" and "spin-on low k" are method recitations in a device claimed. "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

With regard to claim 3, Yew et al. discloses the first low k dielectric layer is comprised of an organic dielectric material.

With regard to claim 4, Yew et al. discloses the first low k dielectric layer is selected from the group consisting of: SiLK.

With regard to claim 6, it is inherent that the low k CMP protective layer is covalently bonded to the first low k dielectric layer.

With regard to claim 7, it is inherent that the low k CMP protective layer is comprised a material (FSG, HSQ) with a low CMP polish rate that can be directly polished without scratching or producing other defects.

With regard to claim 8, Yew et al. discloses the low k CMP protective layer (FSG, HSQ) has a dielectric constant of from about 2.2 to about 3.5.

With regard to claim 9, it is inherent that the low k CMP protective layer is inert to chemicals contained in CMP polish slurries.

With regard to claim 15, Yew et al. discloses the CMP protective layer is comprised of a material selected from the group consisting of silsesquioxane (HSQ).

With regard to claim 16, Yew et al. discloses the material has a low dielectric constant and it is inherent that the material has a low CMP polish rate.

With regard to claim 17, it is inherent that the hardmask/CMP polish stop layer is a conventional hardmask/CMP polish stop layer.

With regard to claim 18, Yew et al. discloses the hardmask/CMP polish stop layer is comprised of silicon nitride.

With regard to claim 19, Yew et al. discloses the first low-k dielectric is an organic dielectric and the low-k CMP protective layer is an inorganic material.

With regard to claim 21, Yew et al. discloses the first low k dielectric is a stack of dielectric containing an embedded etch stop (208).

With regard to claim 25, Yew et al. discloses the structure further comprising a stack of dielectric layers on the substrate, the stack including at least the first low-k dielectric layer and the low k CMP protective layer.

With regard to claim 26, Yew et al. discloses the structure further comprising: a plurality of patterned metal conductors (224,226) formed within the stack of the first low-k dielectric layer and the low-k CMP protective layer.

With regard to claim 27, Yew et al. discloses at least one of the patterned metal conductors (224) is an electrical via.

With regard to claim 28, Yew et al. discloses at least one of the patterned metal conductors (224) is a line connected to the via.

With regard to claim 29, Yew et al. discloses the structure further comprising: a single level of patterned metal conductors (224,226) formed with the stack of dielectric layers on the substrate.

With regard to claim 30, Yew et al. discloses the pattern metal conductor (224,226) is a line.

With regard to claim 31, Yew et al. discloses the pattern metal conductor (224) is a via

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. (PN 6,265,780) in view of Chooi et al. (PN 6,683,002).

With regard to claim 20, Yew et al. discloses the claimed invention including the interconnect structure as recited in the rejection above. Yew et al. further discloses the low k dielectric layer is SiLK. Yew et al. does not disclose the low k dielectric layer is porous. However, Chooi et al. discloses the low k dielectric layer (16,18) is SiLK or porous. Note Col. 3, lines 1-20 of Chooi et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the low k dielectric layer of Yew et al. being porous, such as taught by Chooi et al. in order to further reduce the dielectric constant of the low k dielectric layer.

With regard to claims 22 and 23, Yew et al. discloses the claimed invention including the interconnect structure as recited in the rejection above. Yew et al. does not teach the thickness of the first low k dielectric layer and the low k CMP protective layer, as that claimed by Applicants. However, Chooi et al. discloses the first low k dielectric layer (16) and the low k CMP protective layer (18) having the thickness as claimed. Note Figures 5 and 8B, and Col. 3, lines 35-69 of Chooi et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first low k dielectric layer and the low k CMP protective layer of Yew et al. having the thickness, such as taught by Chooi et al. since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

With regard to claim 24, Yew et al. discloses the claimed invention including the interconnect structure as recited in the rejection above. Yew et al. further discloses the substrate is a semiconductor wafer. Yew et al. does not teach the substrate having an adhesion promoter layer formed thereon. However, Chooi et al. discloses a substrate having an adhesion promoter layer formed thereon. Note Figures 5 and 8B of Chooi et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the substrate of Yew et al. having an adhesion promoter layer thereon, such as taught by Chooi et al. in order to provide better adhesion between the substrate and the low k dielectric layer.

Allowable Subject Matter

5. Claims 10-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is an examiner's statement of reasons for allowance:

Applicant's claims 10-14 are allowable over the references of record because none of these references disclose or can be combined to yield the claimed interconnect structure comprising the low k CMP protective layer has molecular level free volume or molecular level porosity, as recited in claim 10; the low k CMP protective layer mechanically behaves like a sponge, which provides damping capability under application of down force during polish, as recited in claim 13; and the low k CMP protective layer has fine and evenly dispersed pores, as recited in claim 14.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

December 23, 2004

Hung Vu

Patent Examiner